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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,115	12/15/2003	Fujio Ito	501.37400CV4	4854

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EXAMINER	
CHAMBLISS, ALONZO	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/734,115	ITO ET AL.	
	Examiner	Art Unit	
	Alonzo Chambliss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/369,402.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/5/03, 5/13/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. 09/369,402, filed on 8/6/99.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 12/15/03 and 5/13/05 was filed before the mailing date of the non-final rejection on 6/21/05. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. The formal drawings filed on 12/15/03 have been approved by the examiner.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: "METHOD OF FABRICATING A SEMICONDUCTOR DEVICE UTILIZING LEADS WITH TIPS HAVING A GREATER THICKNESS THAN THE WIDTH ".

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 3-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. In claim 3, the phrase " the lead frame having a plurality of leads and a plate material " is vague and indefinite since it is not clear from the claim how the plate material (i.e. heat radiation plate) is separate from the lead frame.

8. In claim 4, the phrase " the plate material includes a metal plate material includes a metal plate and the tips of the plurality of leads are electrically isolated from the metal plate " is vague in definite since it is not clear from the claim how the leads and the metal plate are electrically isolated when the lead frame includes the leads and the metal plate.

9. In claim 6, the phrase " the plate material of the lead frame has slits " is vague and indefinite since it is not clear from the claim how the lead frame has slits when the written description and the drawings show the slits in the a plate that is separate from the lead frame.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

11. Claims 1 – 7 and 9, insofar as definite, are rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs (US 5,701,034) in view of Yasuhara (US 5,150,193) and Yamauchi (JP 1-309359).

With respect to Claims 1 and 3, Marrs discloses preparing a plurality of leads made of a plate material (see Figs. 2B, 7, and 8) and it is well known in the semiconductor industry that leads are inside lead frame having a framework as evident by Yasuhara (see Figs. 3, 8,17a, and 17b). Preparing a plate 110 (i.e. plate material) including a main surface and a back surface opposite to the main surface, wherein plate 110 having a first portion of the main surface and a second portion of the main surface that is at the outer periphery of the first portion. Preparing a semiconductor chip 101 having a semiconductor element and a plurality of electrodes 115 (i.e. pads) formed on a principal plane. Fastening the semiconductor chip 101 on the first portion of the plate

110. Fastening the tips of leads 102a on the second portion of the plate and after step (e), bonding wires 114 on the tips 102a of the leads 102 and the electrodes 115 of the semiconductor chip 101 to electrically connect to each other. After step (f), sealing the tips 102a of the leads 102, the plate 110, the semiconductor chip 101 and the bonding wires 114 with a molding member 120 (se col. 5 lines 1-33; Figs. 1, 2A, 4, 7, and 8). Marrs fails to disclose wherein the lead have the width of tips of the leads are smaller than the lead thickness of the tips of the leads. However, Yamauchi discloses wherein the leads 2 have the width of tips of the leads are smaller than the lead thickness of the tips of the leads 2 (see English abstract and Figs. 1 and 2). Thus, Marrs and Yamauchi have substantially the same environment of a chip electrically connected to a lead, wherein the chip and portion of the leads are encapsulated. Therefore, one skilled in the art at the time of the invention would readily recognize substituting leads with a width smaller than the thickness of the leads for the leads taught by Marrs, since the leads with the smaller width would occupy a smaller space on the substrate while preventing adjacent leads from contacting one another as taught by Yamauchi.

With respect to Claim 2, Marrs discloses the tips of the lead are separated from each other (see Figs. 2B,3B-3F, 6A, 6B, and 7).

With respect to Claim 4, Marrs discloses wherein the plate material includes a metal plate 110 and the tips of the plurality of leads 102a are electrically isolated from the metal plate by the dielectric layers 206, 208 (see col. 5 lines 59-67 and col. 6 lines 1-15; Figs. 2A and 2B).

With respect to Claim 5, it is well known in the semiconductor industry that bonding wires are made of gold as evident by Yasuhara (see col. 7 lines 16-19).

With respect to Claim 6, Yasuhara discloses wherein the plate material of the lead frame has slits 221 – 224 penetrating the plate material in a thickness direction thereof, wherein the slits 221 – 224 extend closer to the chip mounting area than the tips of the plurality of leads, and wherein the step (b) is performed such that the semiconductor chip 21, 112, is mounted to partially overlap the slits in a plane view (see col. 21 lines 9-29; Figs. 1, 12, 17A, and 17B).

With respect to Claim 7, Yasuhara discloses wherein the plurality of leads of the lead frame is formed by etching (see col. 13 lines 57-60).

With respect to Claim 9, Yasuhara discloses wherein the plurality of leads and the plate material are made of copper (see col. 2 lines 57-61).

12. Claim 8, insofar as definite, is rejected under 35 U.S.C. 103(a) as being unpatentable over Marrs (US 5,701,034), Yasuhara (US 5,150,193), and Yamauchi (JP 1-309359) as applied to claim 3 above, and further in view of Yamada (US 5,939774).

Marrs, Yasuhara, and Yamuchi all fail to disclose wherein the width of each of the plurality of leads is less than 180 um. However, Yamada discloses the width of each of the plurality of leads is less than 180 micrometers as evident by Yamada (see col. 6 lines 56-62). Thus, Marrs, Yasuhara, Yamuchi, and Yamada have substantially the same environment of a lead frame partially encapsulated that is electrically attached to a semiconductor chip. Therefore, it would have been obvious to one skilled in the art at the time of the invention to incorporate a plurality of leads having a width of less than

180 micrometers with the process of Marrs, Yasuhara, Yamuchi, since the leads would facilitate connection for miniaturized semiconductor package while increasing the number of pin connection to the substrate as taught by Yamada.

Double Patenting

13. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

14. Claims 1-9 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 6,803,258. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application and US 6,803,258 both recite a lead frame with leads having a width smaller than the thickness of the tips and a plate that is attached to the leads.

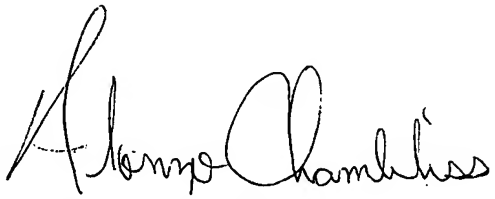
The prior art made of record and not relied upon is cited primarily to show the product of the instant invention.

Conclusion

15. Any inquiry concerning the communication or earlier communications from the examiner should be directed to Alonzo Chambliss whose telephone number is (571) 272-1927.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-7956

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system Status information for published applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PMR only. For more information about the PMR system see http://pair-dkect.uspto.gov. Should you have questions on access to the Private PMR system contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or EBC_Support@uspto.gov.



Alonzo Chambliss
Primary Patent Examiner
Art Unit 2814

AC/June 22, 2005